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| APPLICATION NO.   | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO.   |
|---|-------------|----------------------|---------------------|--------------------|
| 10/528,925  | 09/23/2005  | Steffen Heinz        | 00265P0003 WO US    | 8774               |
| 30996   | 7590        | 12/12/2006           | EXAMINER            |                    |
| ROBERT W. BECKER & ASSOCIATES<br>707 HIGHWAY 333<br>SUITE B<br>TIJERAS, NM 87059-7507 |             |                      |                     | HERNANDEZ, WILLIAM |
| ART UNIT  |             | PAPER NUMBER         |                     |                    |
|   |             |                      |                     | 2816               |

DATE MAILED: 12/12/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

|                              |                        |                     |
|------------------------------|------------------------|---------------------|
| <b>Office Action Summary</b> | <b>Application No.</b> | <b>Applicant(s)</b> |
|                              | 10/528,925             | HEINZ ET AL.        |
|                              | <b>Examiner</b>        | <b>Art Unit</b>     |
|                              | William Hernandez      | 2816                |

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --  
**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

#### Status

- 1) Responsive to communication(s) filed on 23 September 2005.
- 2a) This action is FINAL.                            2b) This action is non-final.
- 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

#### Disposition of Claims

- 4) Claim(s) 10-18 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) Claim(s) \_\_\_\_\_ is/are allowed.
- 6) Claim(s) 10-18 is/are rejected.
- 7) Claim(s) \_\_\_\_\_ is/are objected to.
- 8) Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

#### Application Papers

- 9) The specification is objected to by the Examiner.
- 10) The drawing(s) filed on 23 March 2005 is/are: a) accepted or b) objected to by the Examiner.  
 Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
 Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

#### Priority under 35 U.S.C. § 119

- 12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
  - a) All    b) Some \* c) None of:
    1. Certified copies of the priority documents have been received.
    2. Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
    3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

#### Attachment(s)

- 1) Notice of References Cited (PTO-892)
- 2) Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) Information Disclosure Statement(s) (PTO/SB/08)  
 Paper No(s)/Mail Date \_\_\_\_\_.
- 4) Interview Summary (PTO-413)  
 Paper No(s)/Mail Date. \_\_\_\_\_.
- 5) Notice of Informal Patent Application
- 6) Other: \_\_\_\_\_.

## DETAILED ACTION

### *Drawings*

1. The drawings are objected to because the word "Figur" in Figs. 1-5 should read "Figure". Also, in Fig. 5 the unlabeled rectangular boxes shown in the drawings should be provided with descriptive text labels.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

***Specification***

2. The title of the invention ("Circuit Arrangement For Bridging High Voltages Using a Switching Signal") is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

The following title is suggested: *Level shifter using high voltage capacitors*.

3. The disclosure is objected to because of the following informalities:

All instances of "inlet" and "outlet" should read --input-- and --output--, respectively. Also, all instances of "capacity" and "capacities" should read --capacitance-- and --capacitances--, respectively. This change is needed to conform more closely to conventional terminology in the art.

In line 23 of page 1, the phrase "co-called" should read --so-called--.

4. A substitute specification in proper idiomatic English and in compliance with 37 CFR 1.52(a) and (b) is required. The substitute specification filed must be accompanied by a statement that it contains no new matter.

Appropriate correction is required.

***Claim Objections***

5. Claims 10-13 and 15 are objected to because of the following informalities:

Regarding claims 10-13, all instances of "inlet" and "outlet" should read --input-- and --output--, respectively. This change is needed to conform more closely to terminology conventional to the art.

In line 10 of claim 15, the phrase "push-push" should read --push-pull--.

Appropriate correction is required.

***Claim Rejections - 35 USC § 112***

6. The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

7. Claims 10, 13 and 15 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

8. Regarding claim 1, the phrase "wherein the inlets of the first inverter circuit and the second inverter circuit, respectively, of the voltage transmitter are a non-inverted and an inverted inlet" is not descriptive. None of the figures show the inputs to the inverters as being complementary to each other. Perhaps, Applicant meant to say "non-inverted and an inverted input node/signal".

9. Claim 13 recites the limitation "the third inverter circuit" in line 3. There is insufficient antecedent basis for this limitation in the claim. Perhaps Applicant meant for claim 13 to depend from claim 11 rather than claim 10.

10. Claim 15 recites the limitation "the applied differential principle" in line 9. There is insufficient antecedent basis for this limitation in the claim.

***Claim Rejections - 35 USC § 102***

11. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

12. Claims 10, 14 and 15 are rejected under 35 U.S.C. 102(e) as being anticipated by Tanzawa et al. (USP 6,600,679 B2).

Tanzawa et al.'s Fig. 6 shows a circuit arrangement for bridging high voltages using a switching signal, comprising:

a voltage transmitter with first (V<sub>h</sub>) and second (V<sub>l</sub>) terminals for a low voltage;

a voltage receiver with third (V<sub>H</sub>) and fourth (V<sub>H</sub>) terminals for a higher voltage relative to the low voltage between the first and second terminals, wherein the voltage transmitter and the voltage receiver each comprise a first inverter circuit (I<sub>3</sub> and I<sub>2</sub>, respectively) and a second inverter circuit (I<sub>4</sub> and I<sub>1</sub>, respectively),

wherein the inverter circuits of the voltage transmitter are connected between the first and second terminals and the inverter circuits of the voltage receiver are connected between the third and fourth terminals (clearly shown),

wherein an outlet of the first inverter circuit of the voltage transmitter is connected via a first capacitor (C<sub>1</sub>) as a high voltage capacitor with an inlet of the second inverter circuit of the voltage receiver and an outlet of the first inverter circuit of the voltage receiver, and an outlet of the second inverter circuit of the voltage transmitter is connected via a second capacitor (C<sub>2</sub>) as a high voltage capacitor with an inlet of the

first inverter circuit of the voltage receiver and an outlet of the second inverter circuit of the voltage receiver,

wherein the inlets of the first inverter circuit and the second inverter circuit, respectively, of the voltage transmitter are a non-inverted and an inverted inlet (ND3 is the complement of IN), and wherein the outlets of the first inverter circuit and the second inverter circuit, respectively, of the voltage receiver represent outlet nodes (ND1 and ND2) as called for in claim 10.

As per claim 14, Tanzawa et al. discloses CMOS level circuits (e.g., Fig. 8) for a semiconductor memory device (see title) whose inverters are all CMOS inverters (i.e., complementary transistors connected in series).

As per claim 15, this claim is merely the functionality of the circuit having structure recited in claim 10. Since Tanzawa et al. teaches the structure, the function of the circuit is inherently disclosed.

#### ***Claim Rejections - 35 USC § 103***

13. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

14. Claims 11-13 and 16-18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tanzawa et al. (USP 6,600,679 B2).

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Tanzawa et al. discloses the invention set forth in claim 10 but does not show additional inverters coupled to the inputs of the inverter circuits of the voltage transmitter as called for in claims 11 and 13. However, it is old and well known in the art that adding inverters to the input can be used to control the delay of the circuit. Therefore, it would have been obvious to a person skilled in the art at the time the invention was made to couple a third inverter in series with the first voltage transmitter inverter and a sixth and seventh inverter in series with the second voltage transmitter inverter for the purpose of controlling the circuit's delay for a particular application.

Tanzawa et al. discloses the invention set forth in claim 10 but does not show additional inverters coupled to the outputs of the inverter circuits of the voltage receiver as called for in claim 12. However, it is old and well known in the art that adding an inverter to the output can help in driving the output signal. Therefore, it would have been obvious to a person skilled in the art at the time the invention was made to couple a fourth inverter and sixth inverter to the outputs of the voltage receiver for the purpose of providing gain to the output signal.

Tanzawa et al. discloses the invention set forth in claim 10 but does not show the circuit arrangement packaged as an integrated semi-conductor as called for in claims 16-18. However, it is old and well known in the art that integrating circuits on a semiconductor chip has numerous advantages. Therefore, it would have been obvious to a person skilled in the art at the time the invention was made to realize Tanzawa et al.'s level shifter as an integrated semi-conductor circuit for the purpose of smaller size and lower cost.

***Conclusion***

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to William Hernandez whose telephone number is (571) 272-8979. The examiner can normally be reached on Mon.-Fri. 8:30AM-5:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy P. Callahan can be reached on (571) 272-1740. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

  
TUAN T. LAM  
PRIMARY EXAMINER

WH

WT 12/7/06